AMENDMENTS TO THE CLAIMS:

Please cancel claim 20 without prejudice.

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Previously Presented) A process for connecting processed semiconductor wafers, wherein at least two wafers are located in a mid position of a stack of wafers, and wherein in an operation of a mechanical connecting, electrically insulating connections and electrically conductive connections are produced between at least two semiconductor wafers, said process comprising:

applying structured layers of electrically non-conducting and electrically conducting glass paste on two wafer sides of said two wafers to be connected;

conditioning and premelting of the glass pastes;

geometrical alignment of the two wafers to be connected;

joining the wafers at a processing temperature of the glass pastes using a mechanical pressure.

2. (Previously Presented) The process according to claim 1, wherein the glass pastes are applied by a screen printing process.

3. (Previously Presented) The process according to claim 1, wherein that the non-conducting glass paste and the electrically conducting glass paste have different conditioning and premelting conditions and therefore conditioning and premelting are implemented successively, each in a in a separate process.

4. (Previously Presented) The process according to claim 1, wherein that the non-conducting glass paste and the electrically conducting glass paste have substantially the same processing temperature.

5. (Previously Presented) The process according to claim 1, wherein the non-conductive glass paste and the electrically conducting glass paste have different processing temperatures and these are successively passed in a process.

6. (Previously Presented) The process according to claim 1, wherein at least one of the two wafers is electrically connected in an area that is not structured electronically as an area of a starting material of the wafer.

7. (Previously Presented) The process according to claim 1, wherein the wafers are electrically connected at specific electric circuit points in electronically structured areas.

8. (Previously Presented) The process according to claim 1, wherein a connection formation of the glass pastes takes place at a temperature in a range of 450°C.

9. (Previously Presented) The process according to claim 1, wherein the electric connection of a substrate of an SOI wafer is implemented through previously produced openings in a buried oxide layer and in an active silicon layer.

10. (Cancelled)

11. (Withdrawn) A process for bonding processed semiconductor wafers as system wafer supporting micro-electromechanical or electronic structures with a cover wafer also supporting electronic structures, wherein in an operation of bonding, electrically insulating connections and electrically conductive connections are produced between the semiconductor wafers, said process comprising:

applying a first electrically non-conducting, structured layer and a second electrically conducting structured layer, each one with a glass paste on at least one face of the wafers to be bonded together,

conditioning of the glass pastes;

geometrical alignment of the wafers to be bonded;

joining the wafers together at a processing temperature of the glass pastes using a mechanical pressure.

12. (Withdrawn) The process according to claim 11, wherein the glass pastes are applied with a screen printing process.

13. (Withdrawn) The process according to claim 11, wherein the non-conducting glass paste is low-melting and the electrically conducting glass paste has a different premelting condition and premelting of each of the pastes is implemented successively in a separate process.

14. (Withdrawn) The process according to claim 11, wherein the non-conducting glass paste is low-melting and the electrically conducting glass paste has a substantially same processing temperature.

15. (Withdrawn) The process according to claim 11, wherein the non-conducting glass paste is low-melting and the electrically conducting glass paste has a different processing temperatures.

16. (Withdrawn) The process according to claim 11, wherein at least one of the wafers is electrically connected in a wafer area not structured electronically.

17. (Withdrawn) The process according to claim 11, wherein at least one of the wafers is electrically connected at a specific electric circuit point located in an electronically structured area of the wafer.

18. (Withdrawn) The process according to claim 11, wherein a glass paste connection formation takes place at a temperature of less than 450°C.

19. (Withdrawn) The process according to claim 11, wherein the electric connection of a substrate of an SOI wafer is implemented through at least one previously produced opening in a buried oxide layer of said SOI wafer and in an active silicon layer, of said SOI wafer whereby at least one wall area of the at least one opening in the active silicon layer being provided with an insulating layer prior to the electric connection with the conducting glass paste.

20. (Cancelled)